Dr. Ghassem Jaberipur

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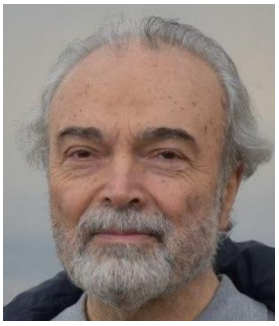

Summary:

Dr. Ghassem Jaberipur, Born in Tehran on the 26th of June 1952, is a graduate of UCLA, UW-Madison, and Sharif University of Technology (SUT). After 43 years of academic life based at Shahid Beheshti University (SBU)[1], he retired on August 23 2022, as a Professor of the Computer Science and Engineering Department, Tehran, Iran. He is currently (as of September, 1st 2022) with the School of IT Convergence Engineering, Chosun University, Gwangju, South Korea, as a Professor for the Brain Pool Program. Besides SBU, he has taught for 4 decades in SUT and Tehran University. In 2016, he received the SUT semi-centennial medal as one of the 50 distinguished SUT graduates for his scientific achievements and services to Iranian society. Dr. Jaberipur's main research is in the field of Computer Arithmetic, for which he received a 2020 international Khwarizmi award.

Education:

- PhD in Computer Engineering, Sharif University of Technology, 2004
- MS in Computer Science, University of Wisconsin in Madison, 1979
- MS in Engineering (Computer Hardware), University of California at Los Angeles, 1976
- BS in Electrical Engineering, Sharif University of Technology, 1974
- High school diploma in Mathematics, Alavi High school, Tehran, 1970

Languages:

Persian (mother tongue)

English (fluent)

French and Arabic (moderate)

German and Spanish (casual)

[1] http://facultymembers.sbu.ac.ir/jaberipur

Professional Experience:

- Professor of the Brain Pool Program, School of IT Convergence Engineering, Chosun University, Gwangju, South Korea (September 2022 - Present)
- Professor, Computer Science and Engineering Department, Shahid Beheshti University, Tehran, Iran (1979 - 2022)
- Visiting Professor, Sharif University of Technology, Tehran, Iran
- Visiting Professor, Tehran University, Tehran, Iran

Research Interests:

Computer Arithmetic, Hardware Accelerators for Artificial Intellegence

Honors and Awards

International Khwarizmi Award (2020)

Semi-centennial medal, Sharif University of Technology (2016)

Brain Pool invited scientist by the National Research Foundation of Korea (NRF), 2022-2024

Publications:

Book Chapter:

Ghassem Jaberipur, "Redundant Number System Based Arithmetic Circuits," in Arithmetic Circuits for DSP Applications, edited by Pramod Kumar Meher and Thanos Stouraitis, published by IEEE & Wiley, 2017

Journals:

1- G. Jaberipur, D. Badri and Jeong-A Lee, "A Parallel Prefix Modulo-$(2^q + 2^{q-1} + 1)$ Adder via Diminished-1 Representation of residues," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 8, pp. 3104-3108, Aug. 2023, doi: 10.1109/TCSII.2023.3256401.

2- Belghadr, A. and G. Jaberipur, "Efficient Variable-Coefficient RNS-FIR Filters with no Restriction on the Moduli Set," *Signal, image and video processing*, *SIViP* 16, 1443–1454 (Sep., 2022). doi.org/10.1007/s11760-021-02097-9.

3- Valavi, M.H, G**.** Jaberipur, K. Al-Rahman Youssefi, "Impact of different types of input wire on defect-tolerance of QCA majority voter," *The European Physical Journal Plus*, (Aug. 27, 2022) 137:977, DOI: 10.1140/epjp/s13360-022-03134-3.

4- Jaberipur, G. and F. Ghazanfari, "Impact of Radix-10 Redundant Digit Set [-6,9] on Basic Decimal Arithmetic Operations," *IEEE Trans. On VLSI Systems*, Vol. 30, Issue 1, pp. 51-59, Jan. 2022, DOI: 10.1109/TVLSI.2021.3120065.

5- Ahmadpour, Z, and G. Jaberipur, "Up to 8k-bit Modular Montgomery Multiplication in Residue Number Systems with Fast 16-bit Residue Channels," *IEEE Transaction on Computer*, Vol. 71, No.6, pp. 1399-1410, June 2021, DOI: 10.1109/TC.2021.3086071.

6- Torabi, Z. G. Jaberipur & S. A. Mirnaseri, "RNS Comparison via Shortcut Mixed Radix Conversion: The Case of Three 4-Moduli Sets $\{2^{n+k}, 2^n \pm 1, m\}$ $(m \in \{2^{n+1} \pm 1, 2^{n-1} - 1\})$," *IETE Journal of Research*, March, 30, 2021, DOI: 10.1080/03772063.2021.1902865

7- Bakhtavari Mamaghani, S., M. H. Moaiyeri, and G. Jaberipur, "Design of an efficient fully nonvolatile and radiation-hardened majority-based magnetic full adder using FinFET/MTJ," *Microelectronics Journal*, vol. 103, p. 104864, Sep. 2020.

8- Hosseini, A., G. Jaberipur, "Complex Exponential Functions: A High-Precision Hardware Realization," *Integration, The VLSI Journal*, Vol. 73, pp. 18–29, July, 2020.

9- Valavi, H., and G. Jaberipur, "Physically Unclonable Functions Based on Small Delay Defects in QCA," *Semiconductor Science and Technology*, Vol. 35, No. 3, March 2020.

10- Torabi, Z., G. Jaberipur, and A. Belghadr, "Fast Division in the Residue Number System $\{\mathbf{2^n + 1}, \mathbf{2^n}, \mathbf{2^n - 1}\}$ Based On Shortcut Mixed Radix Conversion," *Computers and Electrical Engineering*, Vol. 83, No. 5, May 2020.

11- Jaberipur, G., and B. Nadimi, "Balanced $(3 + 2\log n)\Delta G$ Adders for Moduli Set $\{2^{n+1}, 2^n + 2^{n-1} - 1, 2^{n+1} - 1\}$," *IEEE Trans. On Circuits and systems I*, Vol. 67, No. 4, PP. 1368-1377, April 2020, DOI: 10.1109/TCSI.2019.2959638

12- Parhami, B., D Abedi, and G Jaberipur, "Majority Logic, Its Applications, and Atomic-Scale Embodiments," *Computers and Electrical Engineering*, Vol. 83, No. 5, May 2020.

6- Jaberipur, G., A. Belghadr, and S. Nejati, "Impact of diminished-1 encoding on residue number systems arithmetic units and converters," *Computers and Electrical Engineering*, Vol. 75, pp. 61–76, May. 2019.

7- Jaberipur, G., B. Parhami, and D. Abedi, "Adapting Computer Arithmetic Structures to Sustainable Supercomputing in Low-Power, Majority-Logic Nanotechnologies," *IEEE Trans. On sustainable computing*, Vol. 3, No. 4, pp. 262-273, Dec. 2018, DOI: 10.1109/TSUSC.2018.2811181.

8- A. Belghadr, and G. Jaberipur, "FIR Filter Realization via Deferred End-Around Carry Modular Addition," *IEEE Trans. On Circuits and systems I*, Vol. 65, No. 9, pp. 2878-2888, Sep. 2018, DOI: 10.1109/TCSI.2018.2798595.

9- Saba Amanollahi, and G. Jaberipur, "Extended Redundant-Digit Instruction Set for Energy Efficient Processors," *The ACM Transactions on Embedded Computing Systems*, Vol. 17, No. 3, Article No. 70, June 2018, DOI: 10.1145/3202664.

10- Saba Amanollahi, and G. Jaberipur, "Fast Energy Efficient Radix-16 Sequential Multiplier," *IEEE Embedded Systems Letters*, Vol. 9, Issue 3, pp. 73, 76, June 2017.

11- D. Abedi, G. Jaberipur, "Decimal Full Adders Specially Designed for Quantum-Dot Cellular Automata," *IEEE Trans. On Circuits and systems II*, Vol. 65, No. 1, pp. 106-110, January 2018 DOI: 10.1109/TCSII.2017.2703942.

12- G. Jaberipur, and A. Belghadr, "$(5 + 2logn)\Delta$G diminished-1 modulo-$(2^n + 1)$ unified adder/subtractor with full zero handling," *Computers and Electrical Engineering*, Vol. 61, pp. 95–103, July 2017.

13- M. Sangsefidi, D. Abedi, G. Jaberipur, "Radix-8 Full Adder in QCA with Single Clock-Zone Carry Propagation Delay," *Microprocessors and Microsystems*, vol. 51, no. 1, pp. 176-184, Jun 2017, DOI: 10.1016/j.micpro.2017.04.005.

14- H. Ghassemi and G. Jaberipur, "The Impact of Excess-Modulo Representation of Residues on Modulo-$(2^n - 5)$ Parallel Prefix Addition," *The CSI Journal of Computer Science and Engineering*, Vol. 13, No. 2, pp. 48-53, 2016

15- Saba Amanollahi, and G. Jaberipur, "Architecture-Level Design Space Exploration for Radix-16 Sequential Multipliers," *The CSI Journal of Computer Science and Engineering*, Vol. 7, No. 2 & 4 (b), pp. 24-30, 2016

16- Saba Amanollahi, and G. Jaberipur, "Energy Efficient VLSI Realization of Binary64 Division with Redundant Number Systems," *IEEE Trans. On VLSI Systems*, Vol. 25, No. 3, pp. 954-961, March 2017

17- Gorgin, S. and G. Jaberipur, "Sign-Magnitude Encoding for Efficient VLSI Realization of Decimal Multiplication," *IEEE Trans. On VLSI Systems*, Vol. 25, No. 1, pp. 75-86, 2017.

18- Torabi Z. and G. Jaberipur "Fast Low Energy RNS Comparators for 4-Moduli Sets $\{2^n \pm 1, 2^n, m\}$ with $m \in \{2^{n+1} \pm 1, 2^{n-1} - 1\}$," *Integration, the VLSI Journal*, Vol. 55, September 2016, Pages 155–161

19- Hosseini A. and G. Jaberipur "Decimal Goldschmidt: A Hardware Algorithm for Radix-10 Division," *Computers and Electrical Engineering*, Vol. 53, No. 7, pp. 40-55, July 2016.

20- Dorrigiv M. and G. Jaberipur, "Conditional Speculative Mixed Decimal/Binary Adders via Binary-Coded-Chiliad Encoding," *Computers and Electrical Engineering*, Vol. 50, pp. 39–53, 2016.

21- Hosseini A. and G. Jaberipur "Decimal Square Root: Algorithm and Hardware Implementation," *Circuits, Systems & Signal Processing*, December 2016, Volume 35, Issue 12, pp 4195–4219

22- Torabi Z. and G. Jaberipur "VLSI Realization of Low Power/Cost RNS Comparator via Partitioning the Dynamic Range," *IEEE Trans. On VLSI Systems*, Vol. 24, No. 5, pp. 1849-1857, 2016.

23- Jaberipur, G. and Z. Fatemi Langroudi "$(4 + 2\log n)\Delta G$ Parallel Prefix Modulo-$(2^n - 3)$ Adder via Double Representation of Residues in $[0, 2]$," *IEEE Trans. On Circuits and systems II*, Vol. 62, No. 6, pp. 583-587, June 2015.

24- Abedi, D., G. Jaberipur, and M. Sangsefidi "Coplanar Full Adder in Quantum-Dot Cellular Automata via Clock-Zone Based Crossover," *IEEE Trans. On Nanotechnology*, Vol. 14, No. 3, pp. 119-122, May 2015.

25- Ahmadifar H., and G. Jaberipur "A New Residue Number System with 5-Moduli Set: $\{2^{2q}, 2^q \pm 3, 2^q \pm 1\}$," *The Computer Journal*, Vol 58, No. 7, pp. 1548-1565, July 2015.

26- Gorgin, S. and G. Jaberipur, "Comment on "High Speed Parallel Decimal Multiplication with Redundant Internal Encodings"," *IEEE Trans. on Computers*, Vol. 64, No. 1, pp. 293-294, January 2015.

27- Gorgin, S., G. Jaberipur, and R. Hashemi Asl "Efficient ASIC and FPGA Implementation of Binary-Coded-Decimal Digit-Multipliers," *Springer Circuits, Systems, and Signal Processing*, Vol. 33, No. 12, pp 3883-3899, Dec. 2014.

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29- DorriGiv, M. and G. Jaberipur, "Low Area/Power Decimal Addition with Carry-Select Correction and Carry-Select Sum-digits," *Integration, the VLSI Journal*, Vol. 47, No. 4, pp. 443–451, Sep. 2014.

30- Jaberipur, G. and H. Ahmadifar, "A ROM-less Reverse RNS Converter for Moduli Set $\{2^q \pm 1, 2^q \pm 3\}$," *IET Computer & Digital Techniques*, Vol. 8, No. 1, pp. 11-22, 2014.

31- Pishvaie, A., G. Jaberipur, A. Jahanian, “Redesigned CMOS (4; 2) compressor for fast binary multipliers,” *Canadian Journal of Electrical and Computer Engineering*, Vol. 36, No. 3, pp. 111-115, 2013.
32- Jaberipur, G. and M. Dorrigiv, “Formal Ambiguity-resolving Syntax Definition with Asserted Shift Reduce Sets” *Scientia Iranica*, Vol. 20, No. 6, pp. 1939-1952, 2013.
33- Jaberipur, G. and B. Parhami, “Efficient Realization of Arithmetic Algorithms with Weighted Collections of Posibits and Negabits,” *IET Computers & Digital Techniques*, Vol. 6, No. 5, pp. 259-268, 2012.
34- Pishvaie, A., G. Jaberipur, A. Jahanian, “Improved CMOS (4; 2) Compressor Designs for Parallel Multipliers,” *Computers and Electrical Engineering*, Vol. 38, pp. 1703-1716, 2012.
35- Jaberipur, G., H. Alavi, and S. Nejati, “A Modulo 2^n+1 Multiplier with Faithful Representation of Residues,” *The CSI Journal of Computer Science and Engineering*, Vol. 7, No. 2 & 4 (b), pp. 1-7, 2009 (accepted 7,7,2011).
36- Kaivani, A. and G. Jaberipur, “Decimal CORDIC Rotation based on Selection by Rounding,” *The Computer Journal*, Vol. 54, No. 11, pp. 1798-1809 Nov. 2011.
37- Kaivani, A., A. Hosseiny, G. Jaberipur, “Improving the Speed of Decimal Division,” *IET Computer & Digital Techniques*, Vol. 5, No. 5, pp. 393-404, September 2011.
38- Jaberipur, G., “A Generic Modulo $2^n - 1$ Adder Based on Stored Negabit Representation of Residues,” The CSI Journal of Computer Science and Engineering, Vol. 6, No. 2 & 4 (b), pp. 29-35, 2008 (Accepted 12, 13, 2010).
39- Gorgin, S., and G. Jaberipur, “Design and Synthesis of High Speed Low Power Signed Digit Adders,” *Journal of Iranian Association of Electrical and Electronics Engineering*, Vol. 7, No. 2, pp 7-14, Fall & Winter 2010.
40- Jaberipur, G. and S. Gorgin, “An improved maximally redundant signed digit adder,” *Computers & Electrical Engineering*, Vol. 36, No. 3, pp 491-502, May 2010.
41- Jaberipur, G., B. Parhami and S. Gorgin, "Redundant-Digit Floating-Point Addition Scheme Based on a Stored Rounding Value,*" IEEE Trans. on Computers*, Vol. 59, No. 5, May 2010, pp 694-706.
42- Kaivani, A., G. Jaberipur, “Fully Redundant Decimal Addition and Subtraction Using Stored Unibit Encoding,” *Integration, the VLSI Journal*, Vol. 43, No. 1, January 2010, pp 34-41.
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45- Jaberipur, G. "A One-step modulo 2^n+1 Adder Based on Double-lsb Representation of Residues,” *The CSI Journal on Computer Science and Engineering*, Vol. 4, No. 2&4, 2006. pp 10-16 (published in April 2009).
46- Jaberipur, G. and B. Parhami, "Constant-Time Addition with Hybrid-Redundant Numbers: Theory and Implementations," *Integration, the VLSI Journal*, Vol. 41 No. 1, January 2008, PP. 49–64.
47- Jaberipur, G. and A. Kaivani, "Binary-Coded Decimal (BCD) Digit-Multipliers," *IET Computers, and Digital Techniques*, Vol.1, No. 4, pp. 377-381, July 2007.
48- Jaberipur, G. and B. Parhami, "Stored-Transfer Representations with Weighted Digit-Set Encodings for Ultrahigh-Speed Arithmetic," *IET Circuits, Devices, and Systems*, Vol. 1, No. 1, pp. 102-110, February 2007.

49- Jaberipur, G., B. Parhami, and M. Ghodsi, "An Efficient Universal Addition Scheme for All Hybrid-Redundant Representations with Weighted Bit-Set Encoding," *Journal of VLSI Signal Processing*, Vol. 42, No. 2, pp. 149-158, February 2006. (Reprints available on request from the first author).

50- Jaberipur, G., B. Parhami, and M. Ghodsi, "Weighted Two-Valued Digit-Set Encodings: Unifying Efficient Hardware Representation Schemes for Redundant Number Systems," *IEEE Transaction on Circuits and Systems* I, Vol. 52, No. 7, pp. 1348-1357, July 2005.

51- Jaberipur, G. and M. Ghodsi, "High Radix Signed Digit Number Systems: Implementation Paradigms," *Scientia Iranica*, Volume 10, Number 4, pp. 383-391, October 2003.

52- Jaberipur, G. "پردازش کارآ: نیاز اساسی استاندارد کردن رمز تبادل اطلاعات فارسی", *Gosaresh-Computer*, No. 76, page 19, 1986 (English translation of the title: Efficient Processing: A Central Goal in Standardizing the Persian Information Exchange Code)

53- Jaberipur, G. "یک راه حل ساده برای مرتب کردن اطلاعات فارسی", *Gosaresh-Computer*, No. 74, page 3, 1985 (English translation of the title: A Simple Solution for Sorting Persian Data)

54- Jaberipur, G., "فارسی‌سازی زبان‌های برنامه‌سازی", *Gosaresh-Computer*, No. 68, page 5, 1985 (English translation of the title: Realizing the Persian Version of Programming Languages)

Conferences:

1- Jaberipur, G., S. Gorgin, N. Ahamadian, and Jeong-A Lee, "Modulo-($2^q - 3$) Multiplication with Fully Modular Partial Product Generation and Reduction," to appear in Proc. of the 30nd IEEE Symposium on Computer Arithmetic, Portland, Oregon, USA, 2023.

2- Jaberipur, G. and S. Moradi, "Modulo-($2^n + 3$) Parallel Prefix Addition via Diminished-3 Representation of Residues," *in Proc. of the 26th IEEE Symposium on Computer Arithmetic*, June, 10-12, 2019, Kyoto, Japan.

3- Jaberipur, G., B. Parhami, and D. Abedi, "A Formulation of Fast Carry Chains Suitable for Efficient Implementation with Majority Elements," *in Proc. of the 23nd IEEE Symposium on Computer Arithmetic*, pp. 8-15, July, 10-13, 2016, Santa Clara, CA, USA. doi: 10.1109/ARITH.2016.14

4- Abedi, D. and G. Jaberipur, "Coplanar QCA Serial Adder and Multiplier via Clock-Zone Based Crossovers," *in Proc. Of the 18th CSI International Symposium on Computer Architecture and Digital Systems (CADS2015)*, Tehran, Iran, DOI: 10.1109/CADS.2015.7377791.

5- Fatemi, H. and G. Jaberipur, "Modulo-($2^n - 2^q - 1$) Parallel Prefix Addition via Excess-Modulo Encoding of Residues," *in Proc. of the 22nd IEEE Symposium on Computer Arithmetic*, pp. 121-128, June, 22-24, 2015, Lyon, France.

6- Fatemi, H. and G. Jaberipur, "Double $\{0, 1, 2\}$ representation Modulo-($2^n - 3$) adders," *in Proc. Of the 21st International Conference on Systems, Signals, and Image Processing*, May 12-15, 2014, Duborvnik, Croatia, pp. 119-122.

7- Ahmadifar, A., and G. Jaberipur, "Improved modulo-($2^n \pm 3$) multipliers," *in Proc. Of the 17th CSI International Symposium on Computer Architecture and Digital Systems (CADS2013)*, Tehran, Iran, pp. 31-35.

8- Emami, S., M. Dorrigiv, and G. Jaberipur, "Radix-10 addition with Radix-1000 encoding of decimal operands," *in Proc. Of the 16th CSI International Symposium on Computer Architecture and Digital Systems (CADS2012)*, Shiraz, Iran, pp. 3-9, May 2012.

9- Pishvaie, A., G. Jaberipur, and A. Jahanian,
"طراحی کمپرسور (4:2) CMOS سریع بر پایه دروازه XOR سه ورودی"
in Proc. of 17th CSI Computer Conference, Sharif University of Technology, Tehran, Iran, PP. 300-305, March, 6-8, 2012 (English translation of the title: Design of a Fast (4; 2) Compressor Based on 3-way XOR Gate).

10- Jaberipur, G., B. Parhami, and S. Nejati, "On Building General Modular Adders from Standard Binary Arithmetic Components," *Proc. 45th Asilomar Conf. Signals, Systems, and Computers*, Pacific Grove, CA, pp. 154-159, 6-9 November 2011.
11- Gorgin S. and G. Jaberipur, "A Family of High Radix Signed Digit Adders," *in Proc. of the 20th IEEE Symposium on Computer Arithmetic*, pp. 112-120, July, 25-27, 2011, Tubingen, Germany.
12- Jaberipur, G. and S. Nejati, "Balanced Minimal Latency RNS Addition for Moduli Set $\{2^n - 1, 2^n, 2^n + 1\}$," *in Proc. Of the 18th International Conference on Systems, Signals, and Image Processing*, PP. 159-165, 16-18, June 2011, Bosnia and Herzegovina.
13- Jaberipur, G. and B. Parhami, "Posibits, Negabits, and Their Mixed Use in Efficient Realization of Arithmetic Algorithms", *in Proc. Of the 15th CSI International Symposium on Computer Architecture and Digital Systems (CADS2010)*, pp. 3-9, Sep. 23-24, 2010.
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16- Gorgin S. and G. Jaberipur, "Fully Redundant Decimal Arithmetic," *in Proc. of 19th IEEE Symposium on Computer Arithmetic*, pp. 145-152, Jun. 8-10, 2009, Portland, USA.
17- Jaberipur G. and S. Gorgin, "A High Speed Low Power Signed Digit Adder," *in Proc. Of the 16th Iranian Conference on Electrical Engineering*, Tarbiat Modares University, Tehran, Iran, May 13-15, 2008.
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19- Sheikhattar H., V. Rahiman, G. Jaberipur and N. Noroozi, "Design and Implementation issues for the MobFish," *The Twelfth International Conference on Distributed Multimedia Systems*, Grand Canyon, USA, Aug. 30, Sep. 1, 2006.
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22- M. Ghodsi, G. Jaberipur and R. Khosravi, "SADL: A Systolic Array Description Language," Proceedings of 4th CSI Computer Conference (CSICC'98), Sharif University of Technology, Jan. 1999. (in Persian)

Reviewing services for:

- ✓ IEEE Transactions on Computers
- ✓ IEEE Transactions on Circuits and Systems I & II
- ✓ IEEE Transactions on VLSI Systems
- ✓ IEEE Transactions on Information Theory
- ✓ IEEE Access
- ✓ IEEE Signal Processing Letters
- ✓ Integration, the VLSI Journal (Elsevier)
- ✓ Micro Electronics Journal (Elsevier)
- ✓ The Computer Journal
- ✓ 20th IEEE Symposium on Computer Arithmetic
- ✓ Computer & Electrical Engineering (Elsevier)
- ✓ International Journal of Electronics (Taylor&Francis)

Teaching

a) *Graduate courses:*

i. Shahid Beheshti University (SBU):
Advanced Compiler Construction
Computer Arithmetic
Advanced Computer Arithmetic
Division algorithms and hardware
Fault Tolerant Systems
GPU Programming
Decimal Computer Arithmetic
Residue Number Systems

ii. Sharif University of Technology (SUT):
Computational Complexity
Computer Arithmetic

iii. School of Computer Sciences, University of Tehran:
Advanced Compiler Construction

b) Student supervision:

- MS:
  i. Graduated:
  2006: H. Sheikh Attar, M. Asrar Haghighi, A. Abdolalipur, A. Tafakh
  2007: Amir Kaivani
  2008: Hanieh Alavi, Adel Hosseini, Marzieh Moemen
  2009: Marzyeh Tabatabaei
  2010: Morteza Dorrigiv, Saeed Nejati
  2011: Samaneh Emami, Mohammad Mehdi Rasaeizadeh, Ali Motamedi
  2012: Roya Manoochehri, Marzieh Barzegar, Sadegh Nejatzadeh, Mohammad Hassan Fardad
  2013: Hamed Fatemi, Reza Hashemi
  2014: Farzaneh Kargar, Zahra Esmaeilpur, Mona Gharaei, Ehsan Mihandoost
  2015: Dariush Abedi, Kimia Zamiri
  2016: Nasim Shafiei, Majid Jouybari, Hasan Ghasemi Motlagh
  2017: Mostafa Mokhayarn, Seyedeh Atefeh Mirnaseri
  2019: Sahar Moradi
  2020: Bardia Nadimi (co-supervised)
  2021: Tara Nourivandi, Karo Abdollahi, Dariush Badri, Negin Mashayekhi, Sina Bakhtavari
  ii. Withdrawn: Hossein Ghezlseflu, Kamran Hayati
  iii. Current: Roghayeh Kazemi, Mahdieh Haidari, Bardia Elahidoost
- PhD:
  i. Graduated:
  2010: Saeid Gorgin, Amir Kaivani
  2012: Abdolreza Pishvaei
  2013: Hamidreza Ahmadifar
  2016: Morteza Dorri Giv, Zeinab Torabi, Adel Hosseini Hoolari
  2017: Saba Amanollahi
  2019: Armin Belghadr
  2021: Hadi Valavi

ii. Current:

Zabih Ahmadpour, Farzad Ghazanfari, Dariush Abedi, Ramin Hajizadeh, Maryam Norouzi, Elham Rahman, Marzieh Morshedzadeh

c) *Undergraduate courses:*

i. SBU:

- Compiler Construction (ECE, CS, CSE)
- Design, and Implementation of Programming Languages (ECE, CS)
- Automata Theory and Languages (ECE, CS, CSE)
- Operating Systems (ECE)
- Logical Circuits (ECE)
- Data Structures (ECE)

ii. SUT:

- Introduction to Computer Arithmetic
- Compiler Construction
- Design, and Implementation of Programming Languages
- Automata Theory, and Languages
- Compilers and Automata

iii. Engineering School, University of Tehran

- Compiler Construction
- Design, and Implementation of Programming Languages
- Automata Theory, and Languages

Research

Dr. Jaberipur's research interests include Computer Arithmetic and Compiler Construction. Besides the research projects carried out in Shahid Beheshti University (listed below), he is also affiliated to IPM School of Computer Science as a part time researcher.

- Design and implementation of modulo $2^n \pm 1$ adder with stored representation of residues, 2008
- Improving the Efficiency of Syntax-Graph Driven Parsers, Shahid Beheshti University, 2006
- Development of Asserted Shift-Reduce Grammars and Parser Generators, Shahid Beheshti University, 2005
- Designing an FFT Co-processor with Deferred Multiplications, Shahid Beheshti University, 2003
- Design and Implementation of a Syntax Graph Parser Generator, Shahid Beheshti University, 2001
- Development of the Theory of Syntax-Graph Driven Parsers, Shahid Beheshti University, 1985
- A Generalization of Carry Save Adders for Higher Radix Multi-Operand Addition, Confidential technical report, Ref. # 1976, Iran Telecommunication Research Centre, 1985.

Off-University services

a) *Computer Systems:*

- Design and Implementation of the Computerized Telephone Information Data base for State Capitals, Iran Telecommunication Research center, 1985
- Design and Implementation of the Educational and Administrative Automation System, Power and Water Institute of Technology, 1978-2002

b) *Academic:*

- Design of Computer Engineering Curriculum for Iranian Universities, Setade-enghelabe-farhangi, 1980-1982
- Design and selection of nation-wide Graduate Exam in Computer Engineering (English, Automata Theory, Compiler Construction, Design and Implementation of Programming Languages), 1995-2009
- Problem design and student training for national, and international Olympiad for informatics, 1994-2009
- Problem design, and contest organizing for the ACM Collegiate Programming Contest in West Asia, Tehran site, 1999-2006
- Development of the strategic plan for the Iranian National Commission for UNESCO, 1995
- Conference participation:
  - Conference on Trans-border Data Flow, Roma, Italy, 1985
  - UNESCO Conference, Informatics for Education, Paris, 1988
  - UNESCO Conference on Tolerance, New Delhi, 1995
  - UNESCO Conference on Ethics of Information and Communications, Mont Carlo, France, 1996

c) *International:*

- Representing the Ministry of higher education in the Regional Informatics Program for South and Central Asia, New Delhi, India, 1985, Maldives, 1987, and Katmandu, Nepal, 1999
- Member of the Iranian Delegation to the 24th, 25th, 26th, 27th, 28th, 29th, and 30th General Conference of UNESCO, Paris, France, 1987-1999
- Member of the Iranian Delegation to the conference for Education, Geneva, Switzerland, September, 1993
- Representing the high council of Informatics in the 12th General Assembly of the International Bureau for Informatics, Roma, Italy, 1984

Positions

a) *Academic:*

- Faculty Member, Department of Computer Engineering, Shahid Beheshti University (SBU), since 1979
- Advisor for SBU teams to ACM collegiate programming contests, 2007-2010
- Director of the Computer Engineering Department of SBU, 1983, 1995-1997, 2004-2007.
- Vice President for Research, SBU, 1983-1986
- Director of the office for monitoring higher education, Ministry of Culture, and Higher Education, 1986-1988
- Representative of the Ministry of Culture, and Higher Education to the High Council of Informatics, 1986-1988
- Advisor to the Minister of Culture, and Higher Education for Informatic Affairs, 1989-1990
- Advisor for research, Iranian National Commission for UNESCO, 1995-1997
- Member of the Scientific Committee of the ACM Collegiate Programming Contest in West Asia, Tehran site, 1999-2006

- Director of Department of Communications, Iranian National Commission for UNESCO, 1996-1997
- Vice dean for research, Faculty of Computer Science and Engineering, SBU, 2016-2018
- Member of National committee for the Olympiad in Informatics, since 1994

b) *International:*

- Scientific Advisor to the Iranian Permanent Delegation to UNESCO, Paris, France, 1990-1994
- Secretary of the Asia-Pacific group of Permanent Delegations to UNESCO, Paris, France, 1992
- International Olympiad of Informatics (IOI):
  - Assistant to the Leader of the Iranian National team to the International Olympiad of Informatics, Setubal, Portugal, 1998
  - Deputy Leader of the Iranian National team to the Central European Olympiad of Informatics, Slovakia, 2002
  - Deputy Leader of the Iranian National team to the International Olympiad of Informatics in: Tampere, Finland, 2001; Young-in, Korea, 2002
  - Leader of the Iranian National team to the Central European Olympiad of Informatics, Munster, Germany, 2003
  - Leader of the Iranian National team to the International Olympiad of Informatics in: Beijing, China, 2000; Athens, Greece, 2004; Nowy Sacz, Poland, 2005; Merida, Mexico, 2006; Zagreb, Croatia, 2007; Cairo, Egypt, 2008 (not attended due to visa rejection); Plovdiv, Bulgaria, 2009. Waterloo, Canada, 2010.
  - Chair of General Assembly of the 29th International Olympiad of Informatics, Tehran, Iran, 2017.